

Claims

- [c1] 1. A method of fabricating a thin film transistor array substrate, comprising the steps of:
- providing a substrate;
 - forming a first patterned metallic layer, a dielectric layer, an amorphous silicon layer, a second patterned metallic layer and a passivation layer over the substrate in sequence, wherein the first patterned metallic layer comprises a plurality of scan lines and a plurality of gates connected to the respective scan lines and the second patterned metallic layer comprises a plurality of data lines and a plurality of source/drains connected to the respective data lines;
 - forming a patterned photoresist layer over the passivation layer, wherein the patterned photoresist layer at least covers the source/drains and its peripheral regions, part of the edges of the patterned photoresist layer has a plurality of thin-out regions with a smaller layer thickness, and each first thin-out region stretches over part of the edge of one source/drain;
 - removing the passivation layer, the amorphous silicon layer and the dielectric layer exposed by the patterned photoresist layer using the patterned photoresist layer as

an etching mask to form a plurality of staircase structure that correspond to the first thin-out regions; and forming a plurality of pixel electrodes over the substrate such that each pixel electrode at least covers one of the staircase structures and electrically connects with one of the source/drains.

[c2] 2. The method of claim 1, wherein the step of forming the patterned photoresist layer comprises:
forming a photoresist layer over the passivation layer;
and
providing a half-tone photomask and performing a front-exposure and development of the photoresist layer using the half-tone photomask, wherein the half-tone photomask has transparent regions, semi-transparent regions and opaque regions, and the first thin-out regions correspond to the semi-transparent regions in the half-tone photomask.

[c3] 3. The method of claim 1, wherein the first patterned metallic layer and the second patterned metallic layer further comprises a plurality of bonding pads connected to the respective terminals of the scan lines and the data lines and each bonding pads has a plurality of vias organized to form an array.

[c4] 4. The method of claim 3, wherein the step of forming

the patterned photoresist layer comprises:
forming a photoresist layer over the passivation layer;
performing a back-exposure of the photoresist layer using the first patterned metallic layer and the second metallic layer as a photomask such that the amount of energy used in the back-exposure is enough just to expose a portion of the photoresist layer;
providing a photomask and performing a front-exposure of the photoresist layer using the photomask such that the amount of energy used in the front-exposure is enough just to expose a portion of the photoresist layer, wherein the photoresist layer above the source/drains within the first thin-out regions are exposed in the front-exposure operation and the remaining areas within the first thin-out regions are exposed in the back-exposure operation; and
developing the photoresist layer.

[c5] 5. The method of claim 4, wherein the metallic layer between neighboring vias has a width smaller than the back-exposure resolution during the back-exposure operation.

[c6] 6. The method of claim 1, wherein the second patterned metallic layer further comprises a plurality of capacitor electrodes located above some of the scan lines and part of the edges of the patterned photoresist layer further

comprises a plurality of second thin-out regions with a smaller layer thickness and each second thin-out region stretches over part of the edge of one capacitor electrode.

- [c7] 7. The method of claim 1, wherein the step of forming the first patterned metallic layer comprises:
forming a first metallic layer over the substrate;
forming a first patterned photoresist layer over the first metallic layer; and
removing a portion of the first metallic layer using the first patterned photoresist layer as an etching mask.
- [c8] 8. The method of claim 1, wherein the step of forming the second patterned metallic layer comprises:
forming a second metallic layer over the amorphous silicon layer;
forming a second patterned photoresist layer over the second metallic layer; and
removing a portion of the second metallic layer using the second patterned photoresist layer as an etching mask.
- [c9] 9. The method of claim 1, wherein after forming the amorphous silicon layer but before forming the second patterned metallic layer, further comprises forming an ohmic contact layer between the amorphous silicon layer and the second patterned metallic layer.

- [c10] 10. The method of claim 1, wherein the step of removing the material layers comprises performing an isotropic etching process.
- [c11] 11. The method of claim 10, wherein the step of removing the material layers comprises performing an etching operation using an etching solution having a greater etching rate on the amorphous silicon layer than the dielectric layer.
- [c12] 12. A method of fabricating a stacked film structure, comprising the steps of:
providing a substrate;
forming a dielectric layer, an amorphous silicon layer, a first patterned metallic layer and a passivation layer over a front surface of the substrate in sequence;
forming a patterned photoresist layer over the passivation layer, wherein part of the edges of the patterned photoresist layer has thin-out regions with a smaller layer thickness and each thin-out region stretches over part of the edges of the first patterned metallic layer;
and
removing the passivation layer, the amorphous silicon layer and the dielectric layer exposed by the patterned photoresist layer using the patterned photoresist layer as an etching mask and removing the passivation layer un-

der the thin-out regions to form staircase structures that correspond to the thin-out regions.

[c13] 13. The method of claim 12, wherein before forming the dielectric layer further comprises forming a second patterned metallic layer and a portion of the second patterned metallic layer is exposed after removing the passivation layer, the amorphous silicon layer and the dielectric layer exposed by the patterned photoresist layer.

[c14] 14. The method of claim 13, wherein the step of forming the patterned photoresist layer comprises:
forming a photoresist layer over the passivation layer;
and
providing a half-tone photomask and using the half-tone photomask to perform a front-exposure of the photoresist layer, wherein the half-tone photomask has transparent regions, semi-transparent regions and opaque regions and the thin-out regions correspond to the semi-transparent regions in the half-tone photomask.

[c15] 15. The method of claim 13, wherein the step of forming the patterned photoresist layer comprises:
forming a photoresist layer over the passivation layer;
performing a back-exposure of the photoresist layer using the first patterned metallic layer as a photomask

such that the amount of energy used in the back-exposure is enough just to expose a portion of the photoresist layer;

providing a photomask and using the photomask to perform a front-exposure of the photoresist layer such that the amount of energy used in the front-exposure is enough just to expose a portion of the photoresist layer, wherein the photoresist layer above the first patterned metallic layer within the thin-out regions are exposed in the front-exposure operation and the areas in the remaining thin-out regions are exposed in the back-exposure operation; and
developing the photoresist layer.

[c16] 16. The method of claim 12, wherein the step of forming the patterned photoresist layer comprises:

forming a photoresist layer over the passivation layer;
and

providing a half-tone photomask and using the half-tone photomask to perform a front-exposure of the photoresist layer, wherein the half-tone photomask has transparent regions, semi-transparent regions and opaque regions and the thin-out regions correspond to the semi-transparent regions in the half-tone photomask.

- [c17] 17. The method of claim 12, wherein the step of forming the patterned photoresist layer comprises:
forming a photoresist layer over the passivation layer;
performing a back-exposure of the photoresist layer using the first patterned metallic layer as a photomask such that the amount of energy used in the back-exposure is enough just to expose a portion of the photoresist layer;
providing a photomask and using the photomask to perform a front-exposure of the photoresist layer such that the amount of energy used in the front-exposure is enough just to expose a portion of the photoresist layer, wherein the photoresist layer above the first patterned metallic layer within the thin-out regions are exposed in the front-exposure operation and the areas in the remaining thin-out regions are exposed in the back-exposure operation; and
developing the photoresist layer.
- [c18] 18. The method of claim 12, wherein the step of removing the material layers comprises performing an isotropic etching process.
- [c19] 19. The method of claim 18, wherein the step of removing the material layers comprises performing an etching operation using an etching solution having a greater etching rate on amorphous silicon than the dielectric

layer.

- [c20] 20. The method of claim 12, wherein after removing a portion of the passivation layer, the amorphous silicon layer and the dielectric layer, further comprises forming a conductive layer over the substrate such that the conductive layer covers the staircase structure.
- [c21] 21. The method of claim 12, wherein after forming the amorphous silicon layer but before forming the first patterned metallic layer, further comprises forming an ohmic contact layer between the amorphous silicon layer and the first patterned metallic layer.